BIAS CIRCUIT HAVING A START-UP CIRCUIT

BACKGROUND OF THE INVENTION

1. Field of the Invention

[01] The present invention relates to a bias circuit having a start-up circuit, and more particularly, to a bias circuit having a start-up circuit, which prevents noise from power source voltage and power consumption due to static currents and is improved in a high frequency range stability. The present application is based on Korean Patent Application No. 2003-11400, which is incorporated herein by reference.

2. Description of the Related Art

[02] In general, various kinds of bias circuits are used upon designing analog circuits, and a start-up circuit is used in such bias circuits in order to prevent transient states occurring at the beginning of a supply of power source voltage. That is, the start-up circuit refers to a circuit that operates only at the beginning of power supply so that a bias circuit generates a stable bias voltage.

[03] FIG. 1 is a view for showing a general bias circuit using the Wilson current mirror. Referring to FIG. 1, a bias circuit has PMOS transistors MP_{11} and MP_{12}, NMOS transistors MP_{13} and MP_{14}, and a resistor R_{11}.

[04] The bias circuit structured as above has two operation states. One of the two operation states is to output a normal bias voltage, and the other state is to perform abnormal operations at the initial time that a power source voltage is applied. That is, when the power source voltage is applied, a node N_{11} at which the gates of the PMOS transistors MP_{11} and MP_{12} are connected has a predetermined power source voltage value, and a node N_{12} has a voltage of "0". The voltage of the node N_{12} is amplified by a predetermined voltage applied through the PMOS transistor MP_{11}. Accordingly, the PMOS transistors MP_{11} and MP_{12} constructing the current mirror maintain a turn-on state due to the voltage of the node N_{11}, and, at this time, if the PMOS transistors MP_{11} and MP_{12} have the same W/L ratio, the same current is applied to NMOS transistors MN_{13} and MN_{14}. A voltage of the node N_{12} applied through the PMOS transistors turns on the NMOS transistors MN_{13} and MN_{14}. In here, if the NMOS transistors MN_{13} and MN_{14} have the same W/L ratio, a current flowing in a resistor R_{11} becomes identical to a current flowing in the NMOS transistor MN_{13}. Through such operations, a normal bias voltage V_{REF} is output through a REF terminal.

[05] However, if the nodes N_{11} and N_{12} have fixed voltages at the initial time that a power source voltage is applied, the NMOS transistors MN_{13} and MN_{14} are turned off to cut off the current flow, which prevents normal voltages from being produced. Accordingly, the start-up circuit is needed to

prevent transient states occurring at the beginning of a supply of power source voltage.

[06] FIG. 2 to FIG. 4 are views for showing bias circuits having conventional start-up circuits.

[07] In FIG. 2, to a bias circuit of FIG. 1 is added a start-up circuit 20 consisting of a resistor R_{12} and a capacitor C_{21}.

[08] In such a circuit configuration, if a node N_{21} is supplied with a voltage enough to turn on an NMOS transistor MN_{23} through a resistor R_{22} and a capacitor C_{21} at the initial state that a power source voltage is supplied, PMOS transistors MP_{21} and MP_{23} and the NMOS transistor MN_{24} are turned on, so that a bias voltage V_{REF} is outputted through an REF terminal. Since the capacitor C_{21} cuts off current flows at the stable state of power source voltage, there exists no loss caused due to static currents.

[09] However, such a circuit has a drawback in that noise existing on a power source voltage and the like is coupled with the bias voltage V_{REF} through the resistor R_{22} and the capacitor C_{21} and thus affect the bias voltage V_{REF}.

[10] FIG. 3 is a view for showing another example of a bias circuit having a conventional start-up circuit. In FIG. 3, a start-up circuit 30 is used in which diode-connected PMOS transistors $MPP_0 \sim MPP_n$ are connected in multiple stages.

[11] In such a circuit configuration, the diode-connected PMOS transistors MPP_0 ~ MPP_n of multiple stages remain in the turn-on state all the time. Therefore, a voltage of a node N_{31} is expressed in Equation 1 as follows:

[Equation 1]

$$V_{N31} = V_{CC} - 2V_{TH}$$

wherein V_{TH} denotes a threshold voltage of a MOS transistor.

[12] Since a voltage of the node N_{31} becomes a gate voltage of a PMOS transistor MP_{33}, a source voltage of the PMOS transistor MP_{33}, that is, a voltage of a node N_{32} satisfies following Equation 2 with the increase of the power source voltage so that the PMOS transistor MP_{33} is turned on.

[Equation 2]

$$V_{N32} > V_{CC} - V_{TH}$$

[13] Therefore, a PMOS transistor MP_{31} and NMOS transistors MN_{33} and MN_{34} are all turned on so that the bias circuit operates its functions in the normal state. At this time, a voltage of a node N_{32} starts falling down since an NMOS transistor MN_{34} is in turn-on state, which turns off the PMOS transistor MP_{33} so that the start-up circuit completes its function, dissatisfying Equation 2.

[14] However, such a circuit configuration has a drawback in that power loss occurs since static currents exist all the time through the PMOS transistors MPP_0 ~ MPP_n in multiple stages.

[15] FIG. 4 is a view for showing still another example of a bias circuit having a conventional start-up circuit. In FIG. 4, a start-up circuit 40 has the gate of an NMOS transistor MNN_0 connected in common to the gates of two PMOS transistors MP_{41} and MP_{42} of the bias circuit. Accordingly, as power is turned on, a voltage of a node N_{41} increases with a supply of the power source voltage. Since an REF terminal has an initial voltage of "0", an NMOS transistor MNN_0 is turned on according to Equation 3 as follows:

[Equation 3]

$$V_{N41} - V_{REF} > (n+1)V_{TH}$$

[16] At this time, all transistors MPP_0 and $MNN_1 \sim MNN_n$ connected in series in the start-up circuit 40 are turned on so that the voltage of a terminal REF, V_{REF}, increases. The increased voltage V_{REF} turns on the NMOS transistors MN_{43} and MN_{44}. Accordingly, the bias circuit enters its normal operation state. Therefore, a difference between the voltage of the N_{41} and the voltage V_{REF} decreases, so the NMOS transistor MNN_0 is turned off according to Equation 4 as follows:

[Equation 4]

$$V_{N41} - V_{REF} < (n+1)V_{TH}$$

[17] Such a circuit configuration performs a function of cutting off static current consumption in the start-up circuit, to thereby reduce power loss, playing a role of suppressing noise from the power source voltage.

[18] However, such a circuit has a structure of connecting two amplifiers in the positive feedback manner, that is, an amplifier of PMOS transistor MP_{41} loading the NMOS transistor MN_{43}, and the other amplifier of NMOS transistor MN_{44} loading the PMOS transistor MP_{42}. An amplification gain of such a feedback loop has a small value in a low frequency range, but can have a large value in a high frequency range due to a load capacitor and the like. Accordingly, the circuit can have a gain value larger than 0dB in a high frequency range, which causes a frequency stability problem of oscillating an output. Such a problem occurs even in the circuits of FIG. 2 and FIG. 3 alike.

[19] FIG. 5A and FIG. 5B are views for showing frequency characteristics of bias circuits having conventional start-up circuits. In FIGS. 5A and 5B, if the gain becomes larger than 0dB in a high frequency range, a phase margin becomes nearly close to 0 or negative (-) at the point that the gain becomes 0dB, but the gain becomes smaller as a load becomes larger.

[20] FIG. 6 is a view for showing the measurements of an output voltage of a bias circuit having a conventional start-up circuit. In FIG. 6, the oscillation of the output voltage can be seen.

[21] Accordingly, as can be seen in FIG. 5A, FIG. 5B, and FIG. 6, the bias circuits having the conventional start-up circuits need to be reviewed in the aspect of stability, and solutions are needed for the stability problems.

SUMMARY OF THE INVENTION

[22] The present invention has been devised to solve the above problems, so it is an aspect of the present invention to provide bias circuits having a start-up circuit which eliminate noise from a power source voltage and power consumption due to static currents and improve stability characteristics in a high frequency range.

[23] In order to achieve the above aspect, a bias circuit having a start-up circuit comprises a bias circuit part using a current mirror circuit, and for generating a constant bias voltage to an output node from an application of a power source voltage, and a start-up circuit part having a capacitor connected between the output node and a common node of in common connecting gates of MOS transistors constructing the current mirror circuit.

[24] The bias circuit part includes a first PMOS transistor having the source thereof connected to the power source voltage; a second PMOS transistor having the gate and drain thereof connected to the gate of the first PMOS transistor to form the common node, and having the source thereof connected to the power source voltage; a first NMOS transistor having the drain and gate thereof connected to the first PMOS transistor to form the output node, and having the source thereof connected to the power source voltage; a second NMOS transistor having the drain thereof connected to the drain of the second PMOS transistor, and having the gate thereof connected to the gate of the first

NMOS transistor; and a resistor connected the source of the second NMOS transistor and the ground.

[25] Further, in order to achieve the above object, a bias circuit having a start-up circuit comprises a bias circuit part using the cascode current mirror circuit of a double-stage current mirror circuit, and for generating a constant bias voltage to an output node from an application of a power source voltage; and a start-up circuit part for actuating the bias circuit part upon an initial application of the power source voltage, the start-up circuit part including a first capacitor connected between a first common node connecting in common the gates of MOS transistors constructing a single-stage current mirror circuit of the cascode current mirror circuit and a second common node connecting in common the gates of MOS transistors constructing the other single-stage current mirror circuit; and a second capacitor connected between the second common node and the output node.

[26] The bias circuit part includes a first PMOS transistor having the gate connected to the power source voltage; a second PMOS transistor having the gate and drain thereof connected to the gate of the first PMOS transistor to form the first common node, and having the source thereof connected to the power source voltage; a third PMOS transistor having the source thereof connected to the drain of the first PMOS transistor; a fourth PMOS transistor having the gate and drain thereof connected to the gate of the first PMOS transistor to form a second common node, and having the source thereof

connected to the drain of the second PMOS transistor; a first NMOS transistor having the drain and gate thereof connected to the drain of the third PMOS transistor to form the output node, and having the source thereof connected to the power source voltage; a second NMOS transistor having the drain thereof connected to the drain of the fourth PMOS transistor, and having the gate thereof connected to the gate of the first NMOS transistor; and a resistor connected between the source of the second NMOS transistor and the power source voltage.

BRIEF DESCRIPTION OF THE DRAWINGS

[27] The invention will be described in detail with reference to the following drawings in which like reference numerals refer to like elements, and wherein:

[28] FIG. 1 is a view for showing a general bias circuit having the Wilson current mirror;

[29] FIG. 2 to FIG. 4 are views for showing bias circuits having conventional start-up circuits;

[30] FIG. 5A and FIG. 5B are views for showing frequency characteristics of a bias circuit having a conventional start-up circuit;

[31] FIG. 6 is a view for showing a waveform of an output voltage of a bias circuit having a conventional start-up circuit;

[32] FIG. 7 is a view for showing a bias circuit having a start-up circuit according to a first embodiment of the present invention;

[33] FIG. 8 is a view for showing an equivalent circuit of FIG. 7;

[34] FIG. 9 is a view for showing frequency characteristics of a bias circuit having a start-up circuit according to a first embodiment of the present invention;

[35] FIG. 10A to FIG. 10C are views for showing waveforms of bias circuits having conventional start-up circuits and start-up circuits according to an illustrative embodiment of the present invention;

[36] FIG. 11 is a view for showing waveforms of output voltages of bias circuits having conventional start-up circuits and start-up circuits according to an illustrative embodiment of the present invention;

[37] FIG. 12 is a view for showing a bias circuit having a start-up circuit according to a second embodiment of the present invention;

[38] FIG. 13 is a view for showing a bias circuit having a start-up circuit according to a third embodiment of the present invention; and

[39] FIG. 14 is a view for showing a bias circuit having a start-up circuit according to a fourth embodiment of the present invention.

DETAILED DESCRIPTION OF THE PREFERRED EMBODIMENTS

[40] Hereinafter, the present invention will be described in detail with reference to the drawings.

[41] FIG. 7 is a view for showing a bias circuit having a start-up circuit according to an embodiment of the present invention. The bias circuit having a present start-up circuit includes a bias circuit having PMOS transistors MP_{71} and MP_{72}, NMOS transistors MN_{73} and MN_{74}, and a resistor R_{71}, and a start-up circuit 70 having a capacitor CP_1.

[42] The gate of the PMOS transistor MP_{71} and the gate and drain of the PMOS transistor MP_{72} are connected in common, and their sources are connected to a power source voltage Vcc respectively, to thereby construct a current mirror circuit. The drains of the PMOS transistors MP_{71} and MP_{72} are connected to the drains of the NMOS transistors MN_{73} and MN_{74}, respectively.

[43] The gate and drain of the NMOS transistor MN_{73} are connected in common to the gate of the NMOS transistor MP_{74} to form an output node, and an output voltage Vgn is outputted through the output node. The sources of the NMOS transistors MN_{73} and MN_{74} are connected to the ground Vss.

[44] The capacitor CP_1 is connected between the output node and a common node to which the gates of the PMOS transistors MP_{71} and MP_{72} constructing the current mirror are connected in common, and plays roles of performing an initial driving of the bias circuit and a frequency compensation.

[45] In such a circuit configuration, a voltage of the node N_{71} before an initial drive voltage is applied can be expressed in Equation 5 as follows.

[Equation 5]

$$V_{N71} < V_{THn}$$

where, V_{TH} denotes a threshold voltage of the MOS transistor.

[46] Since the voltage of the node N_{71} is smaller than V_{THn}, the PMOS transistors MP_{71} and MP_{72} have a turn-off state. In such a state, NMOS transistors MN_{73} and MN_{74} have the turn-off state at the initial time when the power source voltage changes from 0 up to Vcc since its application thereof, so the voltage of the node N_{71} increases in proportion to the power source voltage.

[47] Since the nodes N_{71} and N_{72} are connected to the capacitor CP_1, a voltage of the node N_{71} increases as the voltage of the node N_{72} increases. At this time, the voltage, Vgn, of the node N_{71} continues to increase, and, if a gate voltage of the NMOS transistor MN_{73} becomes higher than the V_{THn}, the NMOS transistor MN_{73} becomes turned-on. Accordingly, consecutively, the NMOS transistor MN_{74} is turned on, and all the PMOS transistors MP_{71} and MP_{72} are turned on, so that a circuit for generating a reference voltage enters a normal operation state.

[48] If the power source voltage becomes completely transient up to the voltage Vcc so as to have a state, the voltages of the nodes N_{71} and N_{72} form

stable bias voltages. At this time, since the capacitor CP_1 is in the open-circuited state with respect to dc currents, no power consumption occurs.

[49] Further, as described above, since such a reference voltage generation circuit has a positive feedback loop formed, the capacitor CP_1 carries out the start-up function together with a function of frequency compensation circuit, so as to play a role of eliminating the possibility of oscillating the reference voltage generation circuit.

[50] FIG. 8 is a view for showing an equivalent circuit of the circuit of FIG. 7. As shown in FIG. 8, the circuit of FIG. 7 can be redrawn to an equivalent circuit with two amplifiers Amp1 and Amp2 of feedback structure and the capacitor CP_1. At this time, the frequency compensation is implemented by the capacitor CP_1, so the oscillation possibility as in the conventional circuit is eliminated.

[51] FIG. 9 is a simulation graph for showing frequency characteristics of a bias circuit having a start-up circuit according to a first embodiment of the present invention. In the graph, the x-axis indicates frequencies and the y-axis shows gains corresponding to the frequencies of the x-axis. As shown in the graph, the frequency compensation is carried out by the capacitor CP_1 so that the gains do not become larger than 0dB even in a high frequency range.

[52] FIG. 10A to FIG. 10C are views for showing output waveforms for a bias circuit having a conventional start-up circuit and a bias circuit having a start-up circuit according to present invention.

[53] FIG. 10A shows an output waveform of a bias circuit having no start-up function, FIG. 10B shows an output waveform of a bias circuit having a conventional start-up circuit, and FIG. 10C shows an output waveform having a start-up circuit according to the present invention.

[54] As shown in the graphs, FIG. 10A shows that a desired bias voltage is not outputted since no start-up function is provided. Further, In FIG. 10B, a desired bias voltage can be outputted with a start-up function provided, but oscillations occur in a high frequency range. However, in FIG. 10C, it can be seen that a stable bias voltage is outputted, but any oscillation phenomenon does not exist with frequencies compensated.

[55] FIG. 11 shows a voltage waveform outputted from a bias circuit having a start-up circuit according to the present invention, and a voltage waveform outputted from a bias circuit having a conventional start-up circuit. In FIG. 11, a waveform A denotes a voltage waveform outputted from the present invention, and a waveform B denotes a voltage waveform of a conventional circuit. As shown in FIG. 11, it can be seen that the output voltage of the bias circuit having the start-up circuit according to the present invention is more stable.

[56] FIG. 12 to FIG. 14 are views for showing diverse circuits formed based on principles according to the present invention.

[57] In FIG. 12, compared to the circuit of FIG. 7, a resistor R_{81} is connected between the source of a PMOS transistor MP_{82} and the power

source voltage, and the entire operations of the circuit with the operations of the current mirror circuit are the same as those of FIG. 7.

[58] FIG. 13 and FIG. 14 show cascade circuits having a current mirror circuit formed in a double stage. A current source circuit has a large small-signal output resistance value so that a current of nearly constant value can be outputted regardless of output voltage value variations. Accordingly, a current source circuit of cascode form is used in order to increase a small-signal output resistance value.

[59] The operation principle of such a circuit, as described in FIG. 7, is to cause capacitors CP_{81}, CP_{91}, CP_{92}, CP_{101}, and CP_{102} used in start-up circuits 80, 90, and 100 to activate the bias circuit upon an initial application of a power source voltage, carrying out a function of frequency compensation.

[60] As aforementioned, the present invention provides a bias circuit having a start-up circuit, which eliminates noise derived from a power source voltage, prevents power consumption due to a start-up circuit, and eliminates the oscillation possibility with stability improved in a high frequency range.

[61] While the invention has been shown and described with reference to a certain preferred embodiment thereof, it will be understood by those skilled in the art that various changes in form and details may be made therein without departing from the spirit and scope of the invention as defined by the appended claims.